High-Voltage Conductivity-Modulated Silicon Rectifier

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Silicon power rectifiers have been made which have reverse breakdown voltages as high as 2,000 volts and forward characteristics comparable to those obtained in much lower voltage devices. It is shown that the magnitude and temperature dependence of the currents can be explained on the basis of space-charge generated current with a trapping level 0.5 eV below the conduction band or above the valence band. The breakdown voltage of a P^+IN^+ diode is computed from avalanche multiplication theory and is shown to be a function of the width of the nearly intrinsic region. A simple diffusion process is evaluated and shown to be adequate for diode fabrication. The characteristics of devices fabricated from high-resistivity compensated, floating-zone refined, and gold-doped silicon are presented. The surface limitation to high inverse voltage rectifiers is discussed.

I INTRODUCTION

The desire for high voltage rectifiers in the electronic industry has pushed the peak inverse voltage of solid state rectifiers to higher and higher values. The purpose of this paper is to present some of the considerations necessary in designing a device with a high inverse voltage and an excellent forward characteristic. In many cases the device characteristics are predictable. Conversely, high voltage diodes are excellent tools for studying many solid state phenomena.

It has been shown[1] that it is possible by the use of the conductivity modulation principle to separate the design of the forward current-voltage characteristic from the reverse current-voltage characteristic of a silicon p-n junction rectifier. Units have been fabricated by the diffusion of boron and phosphorus into high resistivity material, that have reverse breakdown voltages in the range of 1,000 to 2,000 volts.

The reverse currents are of the order of a microampere per square centimeter at room temperature and increase approximately as the square

root of the applied voltage. The magnitude, voltage dependence, and temperature dependence of the reverse currents can be explained as due to space-charge generated current[2] with a trapping level 0.5 eV from either the conduction or valence band. These effects will be discussed in Section II.

In Section III the breakdown voltage and its dependence on the resistivity and width of the high resistivity region of the rectifier will be considered.

In the next section the forward current is discussed and explained by considering both a space-charge region generated current and a diffusion current that takes into account high levels of minority carrier injection.[3]

Device processing information is given in Section V, together with an evaluation of different sources of high resistivity silicon. The devices to be discussed in this paper have been processed with high resistivity p-type material, although some devices have been made with n-type material.

Finally, a discussion of some surface problems associated with high voltage rectifiers is given in Section VI.

Although this paper is entitled "High-Voltage Conductivity-Modulated Silicon Rectifier", the theoretical arguments are applicable to all semiconductor diodes. However, the experimental results have been limited by considering only high voltage diodes.

II REVERSE CURRENT-VOLTAGE CHARACTERISTIC

2.1 Theory

The simple theory[4] for a p-n junction yields an expression for the reverse saturation current density (I_0) which is:

$$I_0 = q\left[n_p\left(\frac{D_n}{\tau_n}\right)^{1/2} + p_n\left(\frac{D_p}{\tau_p}\right)^{1/2}\right], \tag{2-1}$$

where q is the electron charge, n_p is the equilibrium electron density in p-type material, p_n is the equilibrium hole density in n-type material, D_n and D_p are the diffusion constants for electrons and holes, and τ_n and τ_p are the minority carrier lifetimes for electrons and holes.

When reasonable numbers are substituted into (2-1), I_0 at room temperature is of the order of 10^{-10} amperes per square centimeter. This quantity doubles with every increase of 4° C. The theory also contains no voltage dependence of this current. Even when breakdown multiplication[5] is taken into account, there is essentially no voltage dependence

at voltages less than half the breakdown voltage. The magnitude and temperature and voltage dependences of measured diodes do not agree with these theoretical values at room temperatures.

Recently, Pell[6] has shown that the reverse currents at low temperatures in germanium, and at room temperatures in silicon, are dominated by space-charge generated current. The space-charge generated current density (I_{sc}) is given by

$$I_{sc} = q\, W\, G\, M, \tag{2-2}$$

where W is the width of space-charge region, G is the generation rate of hole-electron pairs in the space-charge region, and M is the breakdown multiplication ($M \sim 1$ except near the breakdown voltage). G is given by[2]

$$G = \frac{n_1 p_1}{\tau_{p0} n_1 + \tau_{n0} p_1}, \tag{2-3}$$

where n_1 and p_1 are the densities of electrons and holes respectively if the Fermi levels were at the energy level of the recombination centers, and τ_{n0} and τ_{p0} are the minority carrier lifetimes of electrons and holes respectively in heavily doped p-type and n-type silicon. This expression assumes constant generation over the space-charge region. Thus,

$$n_1 = N_c \exp \frac{q}{kT} (V_r - V_c) = n_i \exp \beta(V_r - V_i), \tag{2-4a}$$

and

$$p_1 = N_v \exp \frac{q}{kT} (V_v - V_r) = n_i \exp - \beta(V_r - V_i), \tag{2-4b}$$

where V_r is the recombination level above the valence band edge V_v, V_i is the midband intrinsic level, $\beta = q/kT$, N_c and N_v are the effective densities of states in the conduction and valence bands $\cong 2.4 \times 10^{19} (T/300)^3$, V_c is the conduction band edge, k is the Boltzmann's constant, and T is the absolute temperature.

Substituting (2-4) into (2-3), one obtains:

$$G = \frac{n_1}{2\sqrt{\tau_{n0}\tau_{p0}}} \frac{1}{\cosh \left[\beta(V_r - V_i) + \frac{1}{2} \ln \frac{\tau_{p0}}{\tau_{n0}} \right]}. \tag{2-5}$$

For the diffused silicon junctions under consideration, it has been found[7] that τ_{n0} equals 1.2×10^{-6} seconds and τ_{p0} equals 0.4×10^{-6} seconds. Also, $n_i = 3.74 \times 10^{15}\ T^{3/2} e^{-6250/T}$ and $V_i = 0.54$ volts. Using these

numbers, (2-6) becomes:

$$G = \frac{1.25 \times 10^{16} \left(\frac{T}{300}\right)^{3/2} e^{20.8(1-300/T)}}{\cosh\left[38.62\left(\frac{300}{T}\right)(V_r - 0.54) - 0.55\right]}, \tag{2-6a}$$

and

$$G = G_{300}(V_r) f(T, V_r), \tag{2-6b}$$

where

$$G_{300}(V_r) = \frac{1.25 \times 10^{16}}{\cosh\left[38.62(V_r - .54) - 0.55\right]}, \tag{2-7a}$$

and (2-7b)

$$f(T, V_r) = \left(\frac{T}{300}\right)^{3/2} e^{20.8(1-300/T)} \frac{\cosh\left[38.62(V_r - 0.54) - 0.55\right]}{\cosh\left[38.62\left(\frac{300}{T}\right)(V_r - 0.54) - 0.55\right]}.$$

In (2-6b), $G_{300}(V_r)$ is the generation rate for a recombination level at V_r equal to 300° K, and $f(T, V_r)$ is the temperature variation of G for a recombination level at V_r normalized to 300° K.

Curves of $f(T, V_r)$ are given in Fig. 1 for several values of V_r with a curve $g(T)$ which is the temperature variation of the reverse saturation current (I_0). Table I gives values for G_{300} for various V_r.

In the reverse biased diffused junctions made with high resistivity material, the junction may be considered abrupt. Therefore, the width (W) of the space-charge region, when the junction is reverse biased to a voltage V, is given by

$$W = \left(\frac{\kappa V}{2qN_A}\right)^{1/2} = 3.14 \times 10^{-5}(V\rho_p)^{1/2} \text{ cm} \tag{2-8}$$

where the units after the first equal sign are electrostatic, and κ is the dielectric constant. In the second expression, V is in volts, and ρ_p, the base material resistivity, expressed in ohm-centimeters. Thus,

$$I_{sc} = 4 \times 10^{-24} G_{300}(V_r) f(T, V_r)[V\rho_p]^{1/2} \text{ amperes-cm}^{-2}. \tag{2-9}$$

It is seen that I_{sc} varies theoretically as the square root of the reverse voltage for values of V less than $\frac{1}{2} V_B$, the breakdown voltage, in which range avalanche multiplication is negligible. The quantity I_{sc} varies inversely with $N_A^{1/2}$ and will be large for high voltage devices with small N_A. The I_{sc} at 300° K for a rectifier with 40 ohm-centimeter base ma-

terial and a reverse bias of 100 volts is given in Table I as a function of V_r. The numbers compare with 8×10^{-10} ampere per square centimeter for I_0. Thus, from diode measurements at room temperature and above, one could not observe V_T less than 0.3 eV from either the conduction or valence band. In fact, from a measurement of the temperature dependence of the reverse currents, one can determine only the recombination level lying closest to the center of the forbidden band. This can be seen more clearly from the following argument: There will be a contribution to the reverse current from the diffusion current $I_{o300}g(T)$ which varies with temperature as $g(T)$. There will be contributions to the reverse cur-

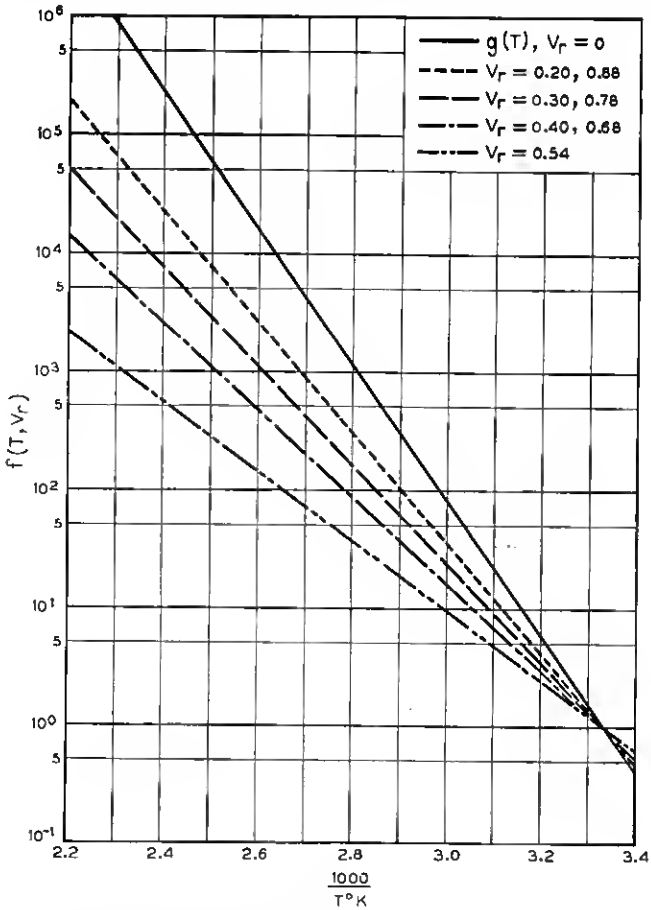

Fig. 1 — The temperature variation of the generation rate, $f(T, V_r)$, for several values of the recombination level, V_r.

TABLE I — VALUES OF G AND SPACE CHARGE GENERATED CURRENT AT 300° K FOR VARIOUS VALUES OF THE TRAPPING LEVEL V_r

$T = 300°$ K $\quad E_g = 1.08eV \quad np = 3 \times 10^{20}$ cm^{-6}

$\tau_{n0} = 1.2 \times 10^{-6}$ sec $\quad \tau_{p0} = 0.4 \times 10^{-6}$ sec

V_r Volts above Valence Band	G_{300} cm^{-3} sec^{-1}	I_{sc} ($V = -100$ volts, $\rho = 40$ ohm-cm) microamperes/cm^2
0.10	5.92×10^{8}	1.88×10^{-7}
0.20	2.84×10^{10}	9.03×10^{-6}
0.30	1.35×10^{12}	4.29×10^{-4}
0.40	6.5×10^{13}	2.06×10^{-2}
0.50	3.02×10^{15}	0.96
0.54	1.08×10^{16}	3.43
0.58	8.1×10^{15}	2.58
0.68	1.95×10^{14}	6.2×10^{-2}
0.78	3.96×10^{12}	1.26×10^{-3}
0.88	8.45×10^{10}	2.69×10^{-5}
0.98	1.78×10^{9}	3.75×10^{-7}

rent by the individual trapping centers given by $I_{sc300}(V_r)f(T, V_r)$, where $I_{sc300}(V_r)$ is the current at 300° K due to generation at recombination centers located at the level V_r, and $f(T, V_r)$ is the temperature variation of the generation rate. Tbus, tbe total reverse current is given by

$$I_{\text{reverse}} = I_{o300}g(T) + \sum_{V_r} I_{sc300}(V_r)f(T, V_r), \tag{2-10}$$

wbere tbe summation is over all recombination levels. The relative currents at 300° K are given in Table I. The greatest contribution at 300° K is due to the level nearest tbe center of the forbidden band. As the temperature increases, all the terms under the summation sign approach each otber. Before a second recombination level contributes significantly to tbe reverse current, bowever, the saturation current will bave become tbe most important component.

2.2 Experimental Results

To evaluate the theory for tbe reverse currents in silicon N^+P junctions, careful measurements were made on five typical units for the reverse current-voltage characteristics at various temperatures from 300° K to 435° K. The curves were taken with a X-Y recorder. The voltage ranged from 0 to 200 volts so that multiplication effects were completely negligible.

From the recorded data, curves of I_r versus $1{,}000/T°$ K were plotted for $V = -10$, -40, and -160 volts. The set of curves for diode No. 3

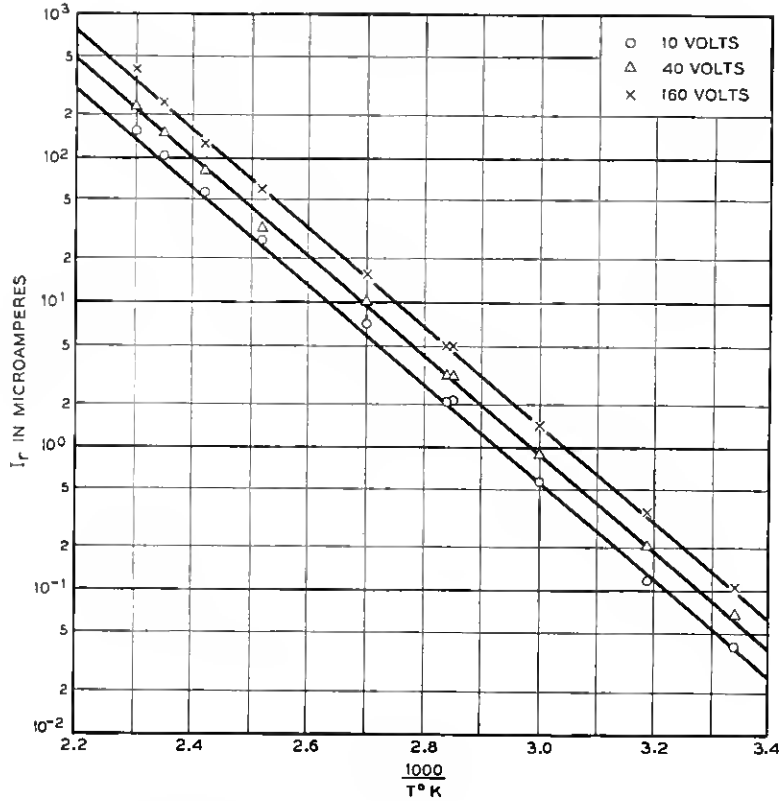

Fig. 2 — The temperature variation of "reverse current" for a typical diode at −10, −40, and −160 volts.

is given in Fig. 2. The slope of these curves indicates that the recombination level lies near 0.5 eV below the conduction band or above the valence band. The junction area of this device is 0.015 cm^2; thus, the current density at 300° K and at −100 volts is 4.4 microamperes per square centimeter. This compares with the order of one microampere as listed in Table I. This suggests that the $(\tau_{n0}\tau_{n0})^{\frac{1}{2}}$ is overestimated. The agreement of this measurement with theory is reasonable.

The voltage variation of the reverse currents does not agree with theory as well as the magnitude and temperature dependence. The experimental results give, as the voltage dependence, an expression:

$$I_r \sim V^{1/N},$$

where N equals 2.9. This compares with the theoretical value of $N = 2$.

Some of this discrepancy can be attributed to the fact that the junction is not truly an abrupt junction. A "graded" junction would yield N equals 3. Measurements of capacitance versus voltage, which essentially measure the width of the space-charge region, yield N equals 2.4. Thus, these devices in the relatively low voltage range still have some contribution from the gradation of the diffused junction.

The highest temperature points in Fig. 2 deviate above the straight lines. This deviation can be attributed to the onset of the contribution from the I_0 component. Calculations indicate that, hy $T = 220°$ C, the contribution to the reverse current hy the space-charge current is equaled by the saturation current and that, hy $T = 320°$ C, the space-charge-generated current is negligible compared to the saturation current.

III BREAKDOWN VOLTAGE OF PN AND PIN JUNCTIONS

3.1 Theory

It has been demonstrated that, in germanium[8, 9] and silicon, reverse biased junctions hreakdown as a result of a solid state analogue of the Townsend β Avalanche Theory. Multiplication and hreakdown occur when electrons or holes are accelerated to energies sufficient to create hole-electron pairs by collisions with valence electrons. Tbe breakdown phenomena in silicon for graded and step junctions has been previously considered.[8, 10] Depending on the impurity distribution, the field in the junction will be a function of distance and will have a maximum value in the region of zero net impurity concentration. The hreakdown voltage is a critical function of the space-charge distrihution.

In this section the existing multiplication theory is extended to the case of PIN junctions. It is shown that relatively wide intrinsic regions are required to obtain breakdown voltages greater than 1000 volts.

Fig. 3 is a plot of the impurity, charge, and field distributions in PIN and PπN junctions. Fig. 3(a) schematically illustrates the geometry of the three region devices considered, and Fig. 3(b) is a plot of the impurity distrihution. In this analysis step junctions will be assumed. For the PIN junction there are no uncompensated impurities in the intrinsic region, and no net charge. At low reverse voltage, the field will sweep through the intrinsic layer and will increase with increasing reverse bias until the hreakdown field is reached.

Absolutely intrinsic material is not yet availahle, and devices are made from high resistivity π-type material. In this class of devices there is some uncompensated impurity and charge in the center region. The field will have a maximum value at the $N^+ \pi$ junction and will decrease

with increasing distance into the π region. At sufficiently high reverse bias the field may sweep into the P^+ region.

Breakdown in silicon[8] is a multiplicative process described by

$$1 - \frac{1}{M} \int_0^W \alpha_1 \, dx, \tag{3-1}$$

where M is the multiplication factor, W is the space-charge width, and α_1 is the rate of ionization which is a strong function of the field in the junction. For a PIN structure, the field is constant, at breakdown M approaches ∞, and

$$\alpha_1 W = 1. \tag{3-2}$$

The ionization rate at breakdown is then a simple function of the width of the intrinsic region. McKay[8] and Wolf[11] have considered α_1 as a func-

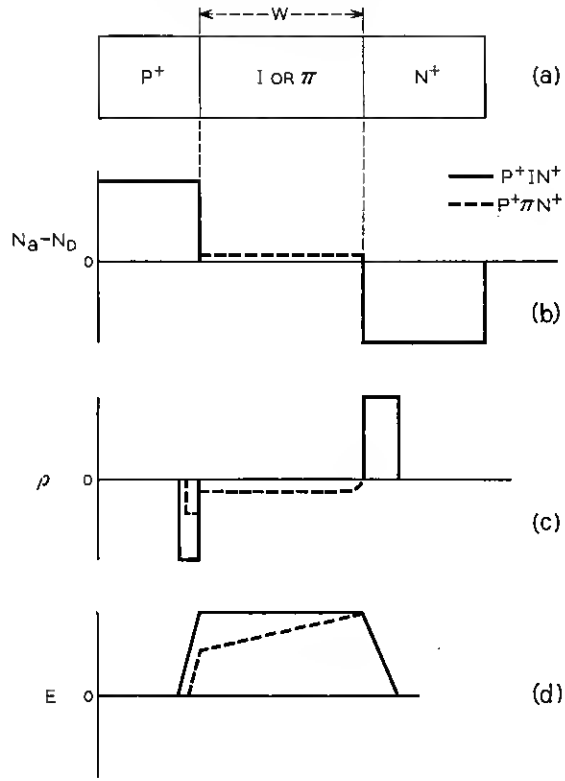

Fig. 3 — Impurity, charge and field distribution in PIN and PπN junctions.

tion of the field. If α_1 is fixed, the field at breakdown can be determined. The breakdown voltage is $\int_0^W Edx$.

Fig. 4 is a plot of breakdown voltage as a function of space-charge width for PN and PIN diodes. The PIN values are calculated; the PN data is previously unpublished data supplied by K. G. McKay.

Some interesting observations can be made from Fig. 4:

I. The plot of breakdown voltage versus barrier width for a PN step junction assumes that the space-charge region does not extend through the high resistivity side of the junction. For this class of junctions the breakdown voltage is determined by the impurity concentration as shown in Fig. 5. The plot of breakdown versus space-charge width for a PIN diode assumes that the space-charge region extends from the P to N region at very low bias, and that it is limited by the width of the I region. If a constant field is assumed in the I region, the breakdown voltage is a function of the barrier width.

2. Although the space-charge region can reach through the I region at low bias, the avalanche breakdown voltage is a function of the width of the I region.

3. For the devices considered here with π regions in the order of 10^{-2} cm, the maximum breakdown voltage is in the order of 2,000 volts.

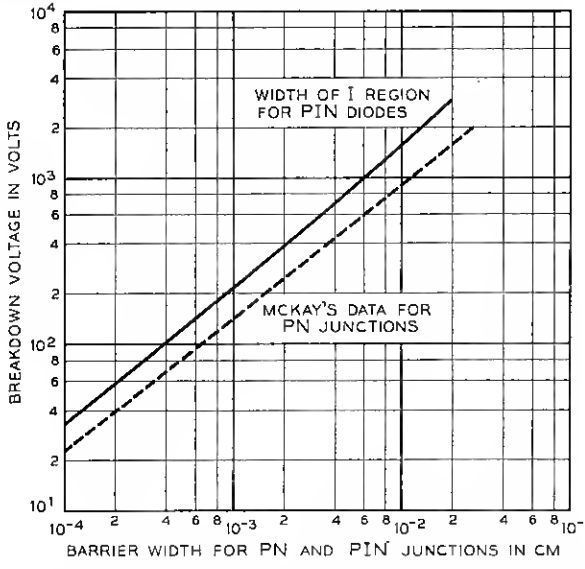

Fig. 4 — Breakdown voltage as a function of barrier width for PN and PIN junctions.

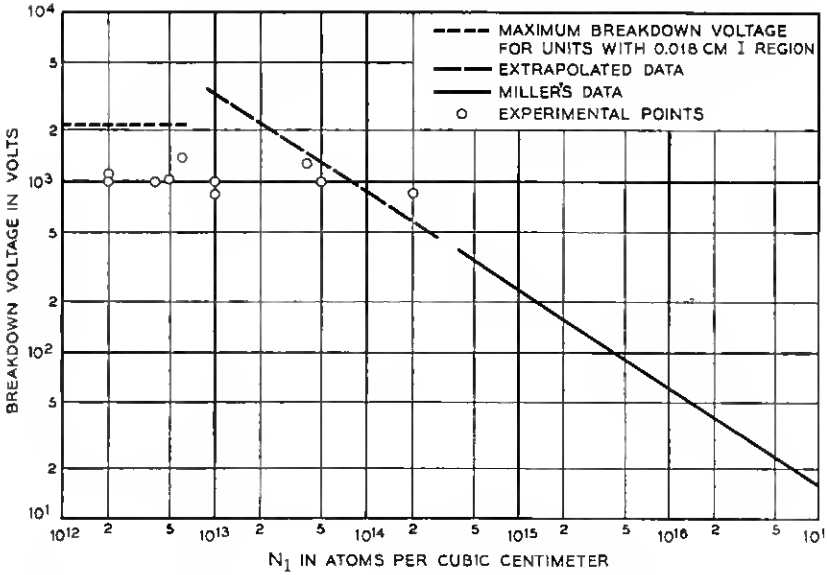

Fig. 5 — Breakdown voltage versus impurity concentration for silicon step junctions.

3.2 Experiment

Fig. 5 is a plot of breakdown voltage versus impurity concentration for silicon step junctions. The plot above 300 volts is extrapolated from the data of Miller[10] and Wilson.[9]

Capacity data, discussed in Section V, indicates that many devices show body breakdown. A few rectifiers break down at voltages as high as 2,000 volts. In many high voltage devices the breakdown voltage is not limited by geometry but by surface problems.

IV FORWARD CURRENT-VOLTAGE CHARACTERISTIC

4.1 Theory

It will be shown in this section that the forward current-voltage characteristic as well as the reverse characteristic can be completely explained by considering both a space-charge region generated current and a diffusion current. The diffusion current component must also take into consideration the effect of high injection levels of minority carriers.

According to the Shockley-Read[2] theory, the rate of recombination, U, of holes and electrons in a semiconductor is given by:

$$U = -G = \frac{pn - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{4-1}$$

where p, and n are the instantaneous concentrations of holes and electrons, respectively. When a PN junction is forward biased, holes and electrons are injected into the space-charge region which has been reduced in width. Some of these carriers diffuse through the space charge region and give rise to the normal diffusion current when the excess minority carriers recombine with majority carriers in field free regions. The other carriers recombine according to (4-1) in the space-charge region giving rise to what is called the space-charge generated current. In the reverse biased junction, the current is due to carriers generated in the space-charge region; whereas, in the forward biased junction, the current is due to recombination of carriers. The quantity U is large in the space-charge region since both p and n are large in this region. In the field free regions, however, one of these quantities is usually small and the product deviates only slightly from n_i^2.

The space-charge generated current, I_{sc}, is given approximately by:[12]

$$I_{sc} = \frac{2qWn_i}{(\tau_{n0}\tau_{p0})^{1/2}} \frac{\sinh \beta \frac{V}{2}}{\beta(V_B - V)} f(b), \tag{4-2}$$

where V_B is the built-in potential of the junction, and $f(b)$ is discussed in Reference 12 and is approximately 1.5 for recombination centers near the intrinsic level as is the case for the diodes under consideration. For shallower recombination levels the function $f(b)$ is much smaller and depends strongly upon the forward applied voltage.

For the forward-biased junction, the space-charge region is narrow, the concentration gradient can be considered linear and W is given by the following expression:[4]

$$W = 4.35 \times 10^2 \left(\frac{V_{\text{junction}}}{\alpha} \right)^{1/3} \text{cm}, \tag{4-3}$$

where V_{junction} is the total potential across the junction in volts and α is the concentration gradient at the junction in cm^{-4}. These are given by:

$$\begin{aligned} V_{\text{junction}} &= V_{\text{built-in}} - V \\ &= kT/q \ln (N_A N_D / n_i^2) - V \\ &= 0.792 - V. \end{aligned} \tag{4-4}$$

$$\text{Also, } \alpha = \frac{C_0}{\sqrt{\pi D t}} e^{-x_j^2/4Dt} \text{ for diffused junctions,} \tag{4-5}$$

where C_0 = surface concentration of diffusant = 3×10^{19} cm^{-3},

D = diffusion constant = 3×10^{-12} cm^2/sec,

t = diffusion time = 5.7×10^4 sec,

x_j = junction depth below surface = 0.003 cm.

When these numbers are substituted into the equations, at 300° K:

$$W = 9.25 \times 10^{-4}(0.792 - V)^{1/3} \text{ cm}. \tag{4-6}$$

For the diodes under consideration:

$$\tau_{n0} = 1.2 \times 10^{-6} \text{ sec}, \qquad \tau_{p0} = 0.4 \times 10^{-6} \text{ sec}.$$

When these expressions are substituted into (4-2), one obtains at 300° C:

$$I_{sc} = 2.8 \times 10^{-7} \frac{\sinh 19.31V}{(0.792 - V)^{2/3}} \text{ amp/cm}^2. \tag{4-7}$$

In order to fit the experimental data, it is necessary to multiply (4-7) by a factor of 5. This may be due to an overestimation of $(\tau_{n0}\tau_{p0})^{\frac{1}{4}}$. Therefore, the equation which shall be used in the remainder of this section will be:

$$I_{sc} = 1.4 \times 10^{-6} \frac{\sinh 19.31V}{(0.792 - V)^{2/3}} \text{ amp/cm}^2. \tag{4-8}$$

A plot of this expression is given in Fig. 6.

The normal diffusion current for low level diffusion,[4] I_{DL}, is given by

$$I_{DL} = I_0(e^{qV/kT} - 1) \tag{4-9}$$

where I_0 is given by (2-1). I_0 for the diodes under discussion is approximately 8×10^{-10} ampere/cm^2 at 300° K. When the injected minority carrier density approaches the equilibrium majority carrier density, the form of (4-9) changes. The high injection level diffusion current, I_{DH}, is then given by[3]

$$I_{DH} = I_{DH0}(e^{qV/2kT} - 1), \tag{4-10}$$

where I_{DH0} equals qn_is/τ, and s equals the width of the high resistivity region. For the diodes under discussion, I_{DH0} is approximately 2×10^{-6} amperes/cm^2 at 300° K. A current-voltage plot of these currents at 300° K for $V_r = 0.50$ is given in Fig. 6 together with their sum. It can be observed that the resulting characteristic starts with slope of qV/kT and bends over to a slope of $qV/2kT$ near 0.10 volt. The slope increases again to near qV/kT at 0.35 volts and decreases once more to $qV/2kT$ above 0.40 volts giving a bump to the over-all characteristic.

Next, consider the temperature dependence of the coefficients of the forward current components

$$I_{sc0} \sim n_i(T), \tag{4-11a}$$

$$I_0 \sim n_i^2 \frac{D_n(T)^{1/2}}{\tau_n(T)} \sim n_i(T)^2, \tag{4-11b}$$

and

$$I_{DH0} \sim \frac{n_i(T)}{\tau(T)} \sim n_i(T). \tag{4-11c}$$

The largest variation of these coefficients is due to the variation of

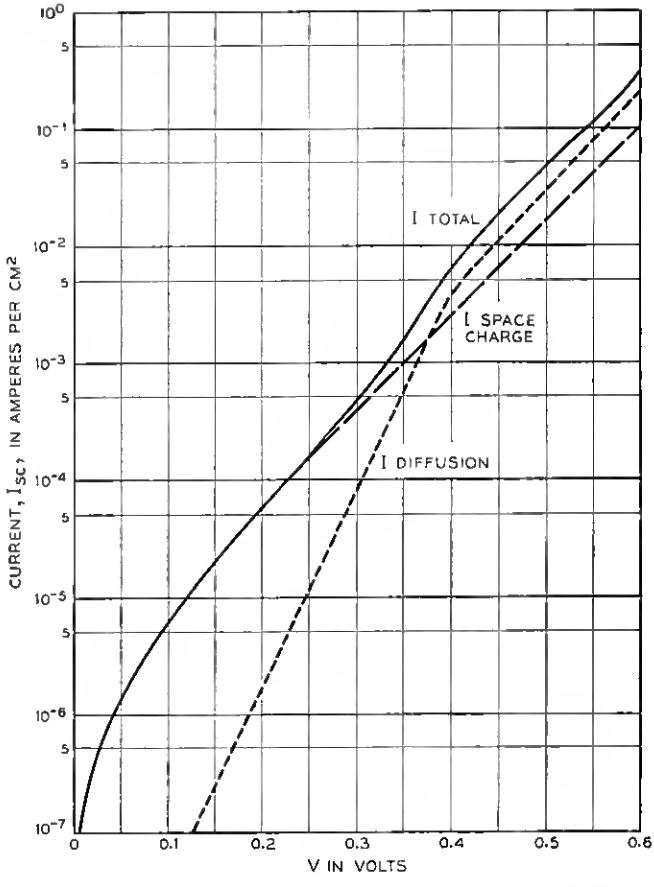

Fig. 6 — The two components of current for a forward biased junction.

n_i with temperature. Fig. 7 gives a plot of this variation. The temperature variations of the otber parameters are all small compared to that of n_i. Thus, as in the case of the reverse currents, at sufficiently high temperatures, the diffusion current makes the more important contribution.

In the case of the forward current, I_{sc} is relatively insensitive to the distribution of impurities; therefore, the results of this section are important for all forward-biased diodes. In high-voltage diodes, to keep the resistive voltage drop small, it is necessary to maintain high minority carrier lifetime in the center region. The diffusion length of injected

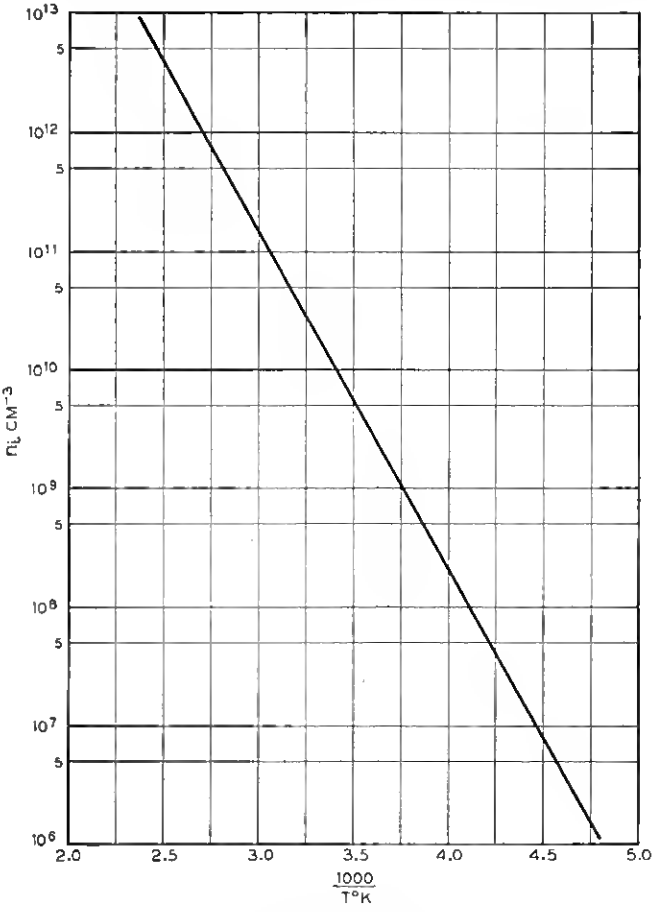

Fig. 7 — The variation of n_i with temperature.

minority carriers should be the order of or larger than the center region width.

4.2 Experimental Results

The forward characteristics of the five typical high voltage rectifiers mentioned in Section 2.2 were measured with a X-Y recorder, and all showed similar shapes. Diode No. 3 will be discussed in detail in this section.

The forward current-voltage characteristic was measured at three temperatures: 220° K, 300° K, and 375° K. Measurements below cur-

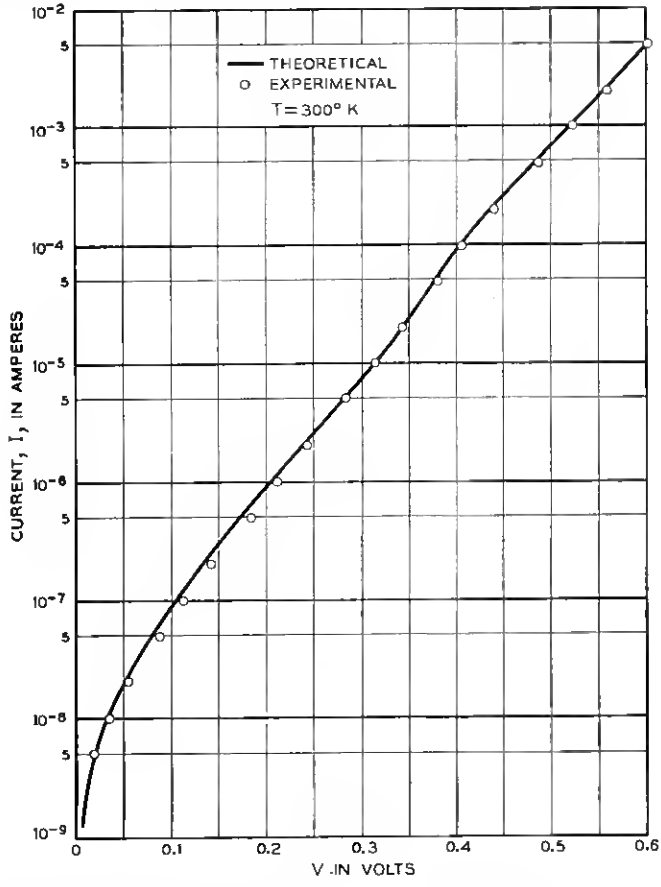

Fig. 8 — The calculated and observed current-voltage characteristic of a forward biased junction at 300° K.

rents of one microampere were made only at 300° K. Currents above 10 milliamperes were not measured since internal power losses would cause temperature variations. The unit has a junction area of 0.015 cm^2, junction lifetime of 4 microseconds at 300° K, S equal to 0.008 cm, and N_A equal to 3×10^{14} cm^{-3}. When these numbers are substituted into the expressions for the coefficients, one obtains, at 300° K,

$$I_{sc0} = 1.4 \times 10^{-8} \text{ amperes},$$

$$I_0 = 1.2 \times 10^{-11} \text{ amperes},$$

$$I_{DH0} = 3.0 \times 10^{-8} \text{ amperes}.$$

Fig. 8 shows a semilogarithmic plot of the current-voltage characteristic at 300° K over a range of $6\frac{1}{2}$ decades. The circles represent measured points and the solid line is the theoretical curve.

Using the variation of n_i given in Fig. 8 and the temperature variations as given in (4-11), one can obtain the coefficients for any temperature. This has been done for two temperatures, 220° K and 375° K. Figs. 9 and 10 show the theoretical and experimental plots at 375° K and 220° K

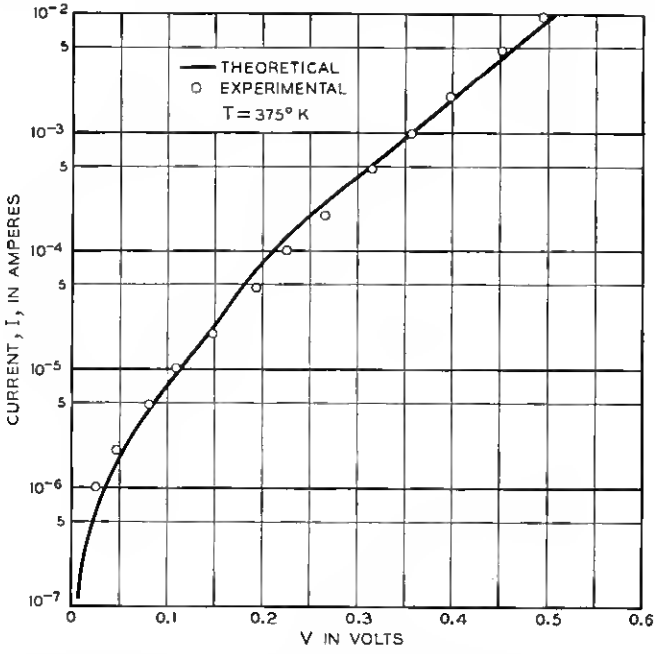

Fig. 9 — The calculated and observed current-voltage characteristic of a forward biased junction at 375° K.

respectively. The circles represent measured points and the solid lines are the calculated theoretical curves. It is observed that the fit in Fig. 9 is quite good; whereas, the fit in Fig. 10 is not as good as at the other temperatures. However, even this figure shows good qualitative agreement of the deviation from a straight line. Some of the factor of two discrepancy in Fig. 10 can be ascribed to the temperature variation of the other parameters, and some to a possible error in the measurement of temperature which would be reflected in the value of n_i.

It should be noted that at all temperatures the IR drop in the high resistivity region is not observable to the limits of the experimental measurements of forward current, 10 milliamperes. This is due to the fact that the region has been conductivity modulated by the forward current. This requires a sufficient minority carrier lifetime in the region so that most of the injected carriers diffuse across the region before recombining. Such lifetimes can be maintained in diffused junctions[7]

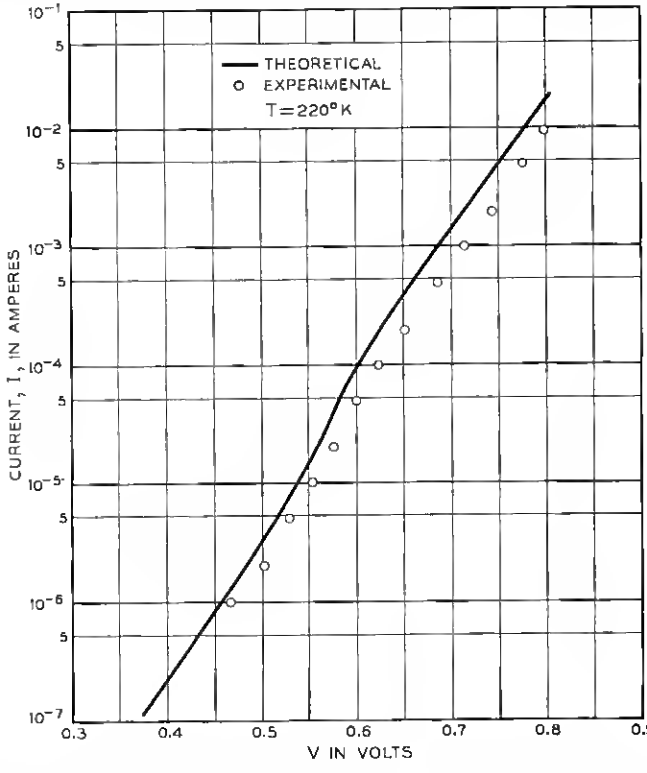

Fig. 10 — The calculated and observed current-voltage characteristic of a forward biased junction at 220° K.

to permit the high resistivity region to be at least as wide as 0.025 centimeters. Thus even in high voltage rectifiers it is still possible to design the forward and reverse current voltage characteristics independently.

V DEVICE PROCESSING

5.1 Silicon Material

Fig. 5 shows that step junctions which break down at over a thousand volts must have a background impurity concentration $\leqq 10^{14}$ atoms/cm^3. The highest grade commercial semiconductor silicon has 5×10^{14} impurities/cm^3 (20–50 Ω cm P type). This material must be processed to reduce the impurity level. To date, high voltage devices have been processed from four types of high resistivity material: floating zone refined, compensated, gold diffused, and horizontal zone refined silicon.

Some silicon was prepared by adding N-type impurities to reduce $| N_D - N_A | < 10^{14}$. Maintaining this delicate balance in material where $N_D \simeq N_A$ is difficult. The boron is relatively uniformly distributed since the distribution constant is close to unity. N-type impurities are less uniformly distributed in the crystal since the distribution constants are considerably less than unity. High resistivity compensated silicon is full of N- and P-region striations. The units processed from this material generally had poor electrical characteristics.

Table II is a typical contour of a compensated crystal. The resistivity varies around the crystal and changes along the length of the crystal. At the bottom of the crystal the resistivity goes through a maximum. The tail end is converted from P to N type.

A number of devices have been fabricated from silicon processed with

TABLE II — A TYPICAL CONTOUR OF A HIGH RESISTIVITY COMPENSATED CRYSTAL
Crystal A-161, Oriented 111, Rotated $\frac{1}{2}$ RPM

Distance from seed (inches)	Resistivity (Ω cm) at Angle				Impurity Type
	0°	90°	180°	270°	
$\frac{1}{2}$	28	33	23	30	P
$\frac{3}{4}$	25	31	31	32	P
$1\frac{1}{2}$	41	22	27	34	P
$1\frac{3}{4}$	57	51	63	37	P
2	160	160	87	200	P
$2\frac{1}{4}$	510	520	—	—	—
$2\frac{1}{2}$	—	—	1200	—	—
$2\frac{3}{4}$	2.9	1.2	0.8	0.8	N

TABLE III — THE CHARACTERISTICS OF SOME HIGH VOLTAGE RECTIFIERS PROCESSED FROM GOLD DIFFUSED AND ZONE REFINED SILICON

Units[1]	E_R (volts)[2]			E_F (volts)[3]			τ (μsec)[4]	Silicon-Type
	10μa	100μa	1 ma	10 ma	100 ma	1 A		
Me-512	30	120	500	0.8	1	1.3	1.6	Gold diffusion $\rho \sim 16{,}000\ \Omega$ cm
513	22	200	600	1.0	1.2	1.5	0.6	
514	300	600	1000	0.8	1	1.5	2.1	
515	300	500	1000	0.8	1	1.4	1.2	
Me-375	1200	1500		2.5	3.5		<1	Floating zone refined $\rho \sim 6{,}000\ \Omega$ cm
376	70	300	800	2.5	4.0		<1	
377	16	120	700	3.5	7			
378	320	400	800	2.5	3.5			

[1] These units have an area $\sim 10^{-3}$ cm^2.
[2] This is the reverse voltage at which these units pass the indicated current.
[3] This is the forward bias at which the units pass the indicated current.
[4] This is the lifetime measured at 30 milliamperes forward current by the pulse injected technique. The lifetime did not seem very sensitive to small variations in injected current.

the floating zone apparatus.[13] This technique removes impurities from molten silicon by treatment with hydrogen containing water vapor. The material obtained from this process has an impurity level in the range of 10^{12} to 5×10^{13} acceptors/cm^3 (2,000 to 16,000 Ω cm P type).

Table III gives the characteristics of some of the better diodes made from such floating zone silicon. The reverse currents are larger than that predicted by (2.10). The lifetime at high injection is in the order of 1 μsec.

N-type silicon with a resistivity range of 10 to 30 Ω cm was diffused with gold at 1,200° for sixteen hours. With this diffusion program the gold is uniformly distributed in the material.[14] The resistivity after gold diffusion was in the range of 2,000 to 15,000 Ω cm. The characteristics of several devices processed from this material are given in Table III. This technique has many attractive features; however, additional work was not done because the lifetime in the diffused material was consistently lower than that required for conductivity modulation.

One successful purification technique is horizontal zone refining of silicon in a quartz boat. With the number of passes used, the background acceptor concentration is observed to be in the order of 5×10^{13} to 10^{14} (100–1,000 Ω cm P type). Most of the devices reported in this paper are fabricated from this material.

Capacity data for devices fabricated from various types of high resistivity silicon is shown in Fig. 11. The plot shows that the high resistivi-

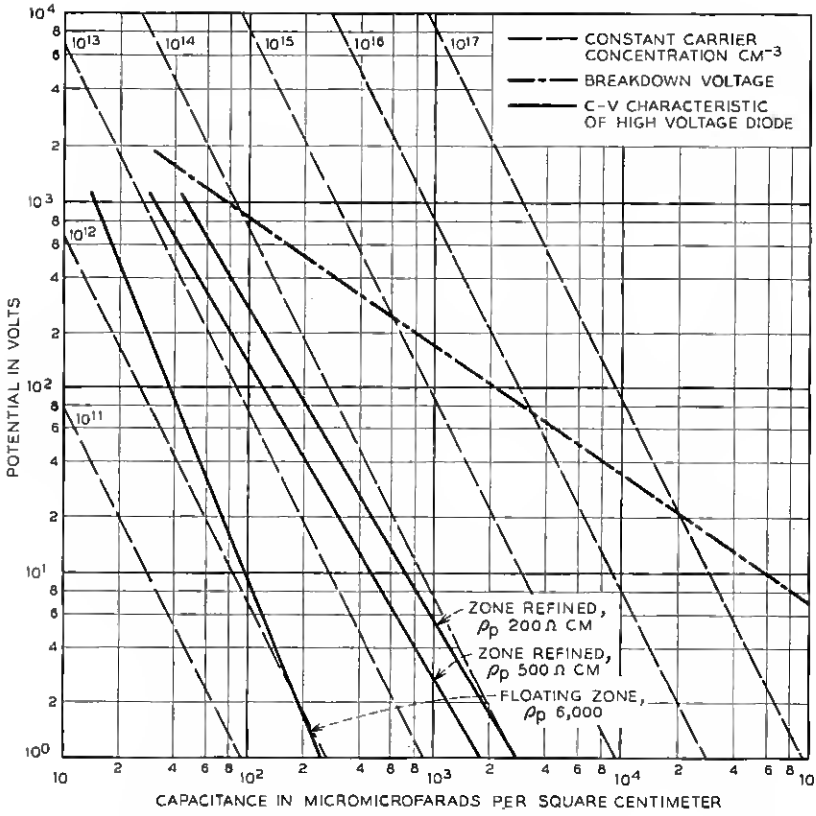

Fig. 11 — Capacity/cm² for high voltage rectifiers processed from various types of high resistivity material.

ties measured by the four point probe before diffusion are indicative of the impurity level after processing. The water vapor floating zone refined material has an impurity level of 10^{12} acceptors/cm^3; the other material is in the range of 10^{13} to 10^{14}. The breakdown voltage line was calculated from the data in Fig. 5.

5.2 Diffusion

In this section some of the practical difficulties observed in utilizing the diffusion technique will be considered. In the fabrication of transistors close geometry control is necessary in order to obtain the desired device characteristic. It has been shown[1] that in conductivity modulated rectifiers the only geometry requirement is that the width of the center

region be less than the diffusion length of the minority carrier. High surface concentration of diffusant is desirable since this facilitates the contact problem. This suggests that the diffusion system can be much less involved than that required for diffused transistors.[15] Some of the data presented in this section will show that the open tube diffusion technique[16] can lead to variations in diffusion parameters.

The diffusion of impurities into silicon is complicated by variations in the boundary conditions at the surface. Frosch[15] has shown that surface concentrations can be varied over six decades.

5.2.1 Device Diffusion Theory

Several important impurity distributions have been considered[17]. Two distributions are important in the open tube process:

1. Error Function Complement, ERFC, Distribution or Infinite Diffusant Source. If the diffusant is deposited on the silicon and serves as an infinite source, the added impurities will have an *erfc* distribution. For one diffusant and a fixed diffusion program this distribution will result in the deepest penetrations and smallest sheet resistanees of all possible distributions. The sheet resistance is a measure of the total number of added impurities. The data presented later indicates that the added impurities frequently have an *erfc* distribution.

2. Gaussian and Modified Gaussian Distribution. A number of impurity atoms enters the solid, and a surface barrier builds up with time which prevents additional atoms from entering.[17] Initially, the diffusant is assumed to be present in an infinitely thin layer at the surface with diffusion into or out of the material possible. In the range of silicon doping levels and surface concentrations used, a Gaussian, modified Gaussian or *erfc* distribution for a given diffusion program lead to approximately equal junction depths.

The sheet resistance and the diffusion depth have been related[18] to the surface concentration for an *erfc* distribution. If the distribution is Gaussian instead of *erfc*, then for the same value of sheet resistance and diffusion depth the surface concentration should be reduced by one-third. Since the sheet resistance is related to the total number of impurities through a mobility term, quantitative interpretation of the data for any case other than *erfc* or Gaussian distributions would be difficult.

5.2.2 Experimental Results

The sheet resistance was measured by the four-point probe method, and the diffusion depths, by angle lapping and staining.[19] Surface con-

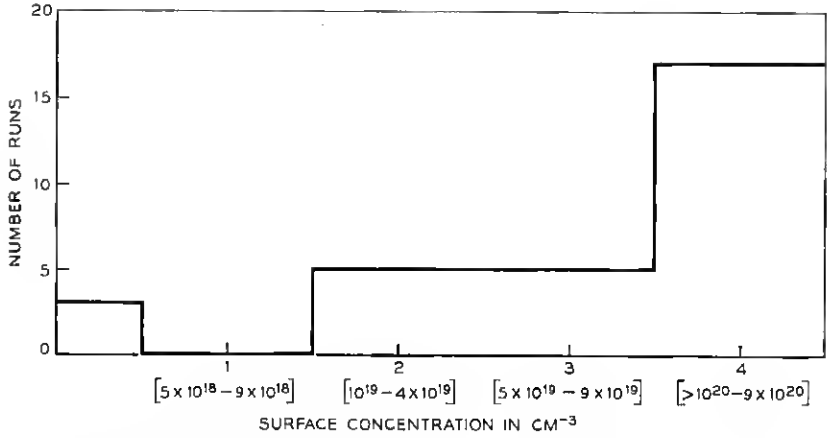

Fig. 12 — Distribution of surface concentration of 28 P_2O_5 diffusions by the open tube deposition technique.

centrations were calculated assuming an *erfc* distribution.[18] All the diffusions are on lapped silicon surfaces in the temperature range of 1,200 to 1,300° C.

Fig. 12 shows the distribution of surface concentration of 28 P_2O_5 diffusions by the open tube process.[16] The surface concentrations vary from 10^{19} to 5×10^{20} atoms/cm^3. These values are about a decade lower than the closed tube values of surface concentrations reported by Fuller.[19]

The measured diffusion depths were in the order of 2×10^{-3} to 5×10^{-3} cm. Fig. 13 shows the distribution of diffusion depths normalized with the calculated diffusion depth as unity. The diffusion depths were calculated from the measured surface concentration assuming an *erfc*[19] distribution.

The observed variation in diffusion depth is difficult to explain. Some of the possibilities which have been considered are:

1. The diffusion temperature from lot to lot would have to be from 0 to 50 degrees below the expected value to explain the variations. Discrepancies this large have not been observed.

2. One impurity distribution which may explain some of the results is a modified Gaussian with considerable out diffusion. There are some runs with high sheet resistance and diffusion depths which are consistent with this picture. Generally the sheet resistances are so small that there could not be much out diffusion.

3. Some workers have suggested the possibility of the diffusion constant being a function of the surface concentration. Fig. 13 does not

indicate any correlation between surface concentration and diffusion constant.

The variations in diffusion process control have not been observed to effect the production of rectifiers. If better geometry control is necessary, more sophisticated diffusion techniques are required.

VI PULSE PROPERTIES AND RELIABILITY

Important considerations in all diode applications are the pulse properties and reliability in operation. In this section some problems which are associated with avalanche breakdown are described and the results related to recent work on surface and body breakdown.

6.1 Theory

Several workers[20] have considered the possibility of a negative resistance in the avalanche region for reverse biased junctions in which one side is either intrinsic or so weakly doped that the space charge of the carriers cannot be neglected. A negative resistance might be observed at very high current densities in an $N^+\pi$ junction.

One possible source of a negative resistance would be a large temperature rise due to current concentration at a few points instead of a uni-

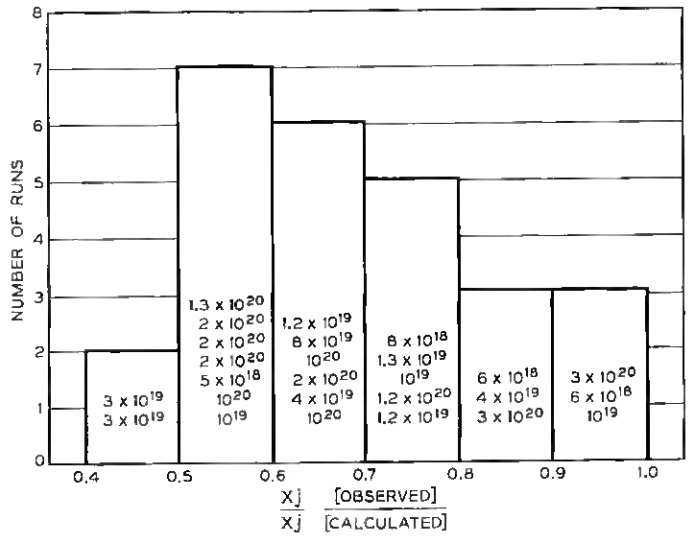

Fig. 13 — Distribution of diffusion depths for diffusion by the open tube deposition technique.

form flow through the junctions. This case is of particular significance in high voltage rectifiers where small reverse currents result in relatively large power. It has been pointed out in Sections 3.2 and 5.1 that body avalanche breakdown is frequently not observed in these devices.

Avalanche breakdown current in silicon[8] is carried by discrete pulses of about 50 μa at their onset and increasing with increasing current to about 100 μa. Approximate calculations[21] show that the ionizing regions of these microplasmas are about 500 Å in extent, have a current density $\approx 2 \times 10^6$ amp/cm^2, and have a net space-charge density $\approx 10^{18}$/cm^3. These pulses for junctions with E_{max} less than 500 kv/cm appear to be independent of junction width and built-in space-charge. Rose considers the statistical problem associated with a large number of pulses and presents a picture which is consistent with most of the experimental data. He calculates the temperature rise, assuming the avalanche power is 1×10^{-2} watts and is dissipated uniformly in a sphere. The maximum temperature rise for a cluster of two or three pulses is in the order of 25° C. For the picture Rose presents, the temperature rise due to the microplasma should be relatively insensitive to the breakdown voltage. Thermal collapse of rectification, i.e., increase of temperature until the silicon is intrinsic, will probably not occur in the region of avalanche multiplication. Two important conclusions can be obtained:

1. Avalanche breakdown should occur as a random process with a uniform probability over the junction. Large temperature rises due to a breakdown of microplasma will probably not occur since the resulting temperature rise would cause the breakdown voltage in that spot to increase. The power is dissipated throughout the path of the current pulse in the space-charge region.

2. A thermal effect in silicon due to heating by the small plasma has a very short time constant of the order of 10^{-10} seconds.[21] It is not possible to separate a thermal effect of this type by reducing the pulse width. The heating and cooling time is short compared to the pulse time in these experiments.

The pulse properties of a junction would be quite different if the breakdown occurred at one spot instead of many spots distributed over the junction. Breakdown at a single spot on the surface has been observed.[22]

6.2 Experimental Results

Many rectifiers were given a voltage pulse which carried them into breakdown. There was a wide distribution of V-I characteristics. Many diodes did not show a negative resistance up to the maximum instan-

taneous power the pulser could deliver, 5kw. These diodes are not considered in the subsequent analysis.

The diodes were subjected to 50 μsec triangular voltage pulses which would send them into breakdown. Variations in pulse conditions did not effect the I-V characteristic until large pulses destructively damaged the unit.

Fig. 14 is a sketch of a typical V-I characteristic and Fig. 15, shows the voltage-versus-time characteristic for a diode with a negative resistance. The V-I curve can be broken into four regions:

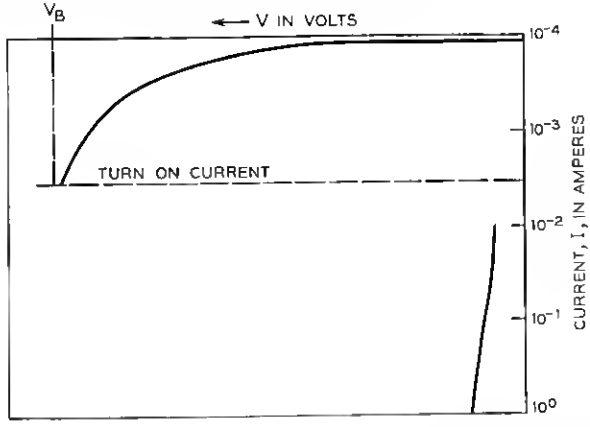

Fig. 14 — A typical V-I characteristic for a diode in which a negative resistance is observed.

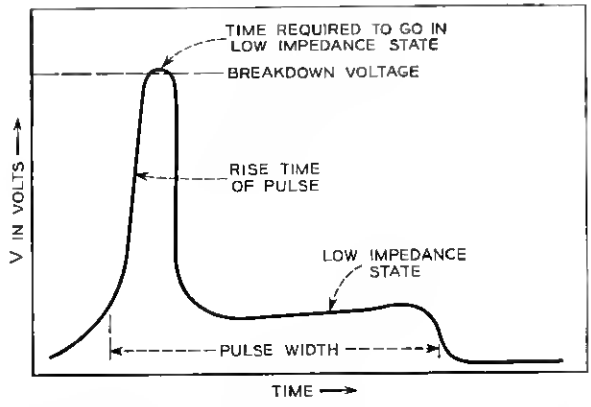

Fig. 15 — A typical V-T characteristic for a diode in which a negative resistance is observed.

1. A high impedance state before the breakdown voltage is reached.
2. A current required to turn on the negative resistance; this current varies from 10^{-3} to 1 amp.
3. The transition to a low impedance state.
4. The low impedance region in which the current is probably limited by the circuit impedance.

The V-T curve can be broken in four regions:

1. The time it takes the pulse to reach the breakdown voltage.
2. The time the diode can maintain the breakdown voltage less than 1 μsec. This is beyond the resolution of the oscilloscope.
3. The time required to fall to the low voltage (low impedance) state, is less than 1 μsec.
4. The remainder of the pulse in the low voltage state.

Fig. 16 is a plot showing the current and voltage required to turn on a negative resistance in several power rectifiers (area $\sim 10^{-2}$ cm^2). To

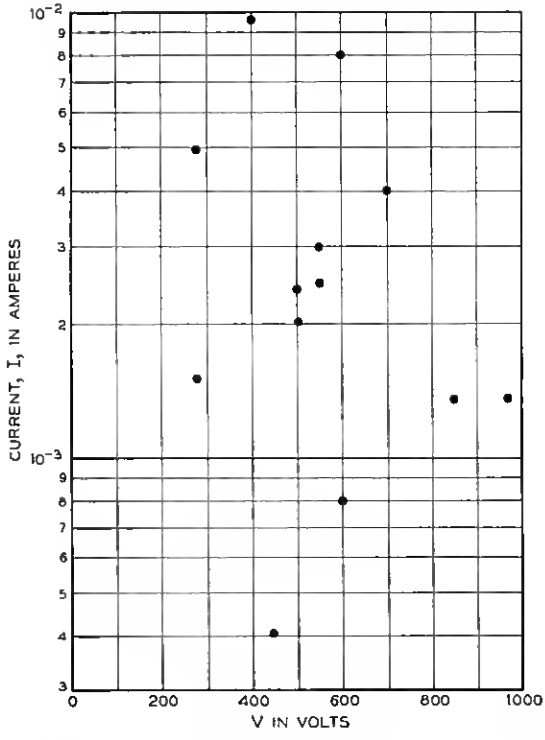

Fig. 16 — Current and voltage required to turn on a negative resistance in several power rectifiers ($A \sim 10^{-2}$ cm^2).

consider the spread of breakdown voltage, the data was normalized to the instantaneous power required to turn on a negative resistance. This turn-on power was the turn-on power multiplied by the voltage.

Fig. 17 is a plot of the distributions of turn-on power for the rectifiers which had a negative resistance plotted as a log normal distribution on probability paper. The median value for the turn-on power is 1.2 watts. Eighty per cent of these diodes went into a negative resistance condition at powers between 0.1 and 10 watts. Many diodes could dissipate several kilowatts with no negative resistance. These were not included.

Experiments show that devices which show surface breakdown will collapse at power levels which are orders of magnitude below that observed for devices in which body breakdown is observed.

The picture is more cloudy with smaller area rectifiers (area $\sim 10^{-3}$ cm^2). In these devices it was not possible to predict the pulse properties

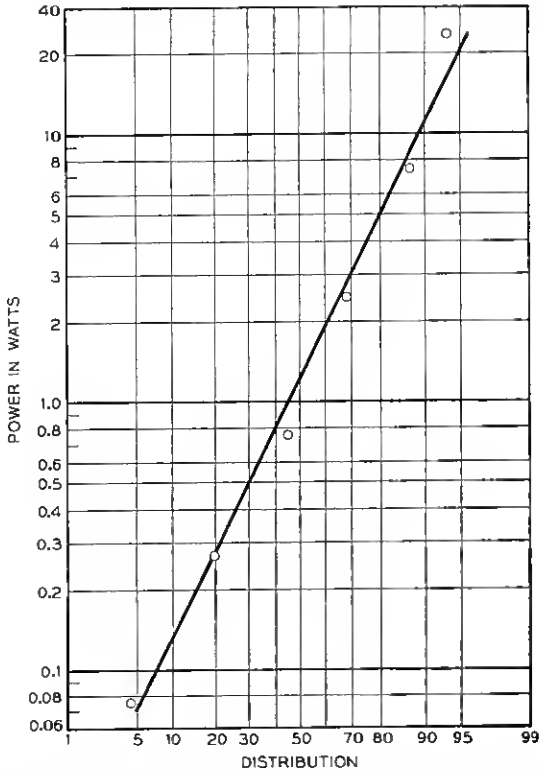

Fig. 17 — The distribution of turn-on power for rectifiers ($A \sim 10^{-2}$ cm^2) in which a negative resistance is observed plotted as a log normal distribution on probability paper.

of the device from the reverse I-V characteristic. This may be attributed to the decrease in power capabilities of the body breakdown process in the smaller devices. This also suggests that the smaller devices have a less severe surface problem.

The distribution of turn-on power for a few hundred small area rectifiers ($A \sim 10^{-3}$ cm^2) is shown in Fig. 18. The median of the distribution occurs at 40 watts. Eighty percent of the units will show a negative resistance when pulsed at power levels between 3 and 500 watts.

VII CONCLUSION

High voltage rectifiers have been fabricated using several sources of high resistivity material employing an uncomplicated diffusion process.

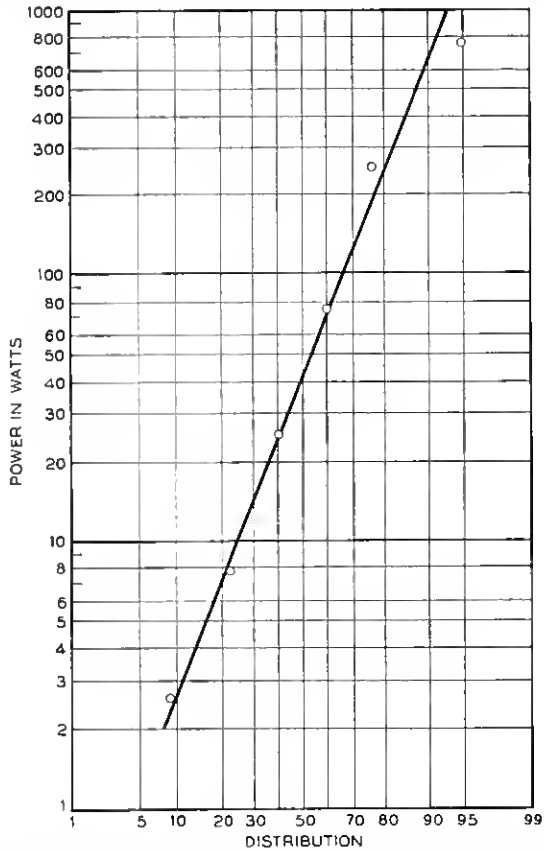

Fig. 18 — The distribution of turn-on power for small area rectifiers ($A \sim 10^{-3}$ cm^2) plotted as a log normal distribution on probability paper.

The most consistent results were obtained using horizontal zone refined silicon. The open tube diffusion technique has sufficient control to satisfy the fabrication requirements.

The magnitudes, voltage and temperature dependences of both the forward and reverse currents of silicon rectifiers can be explained by including a recombination level near the middle of the forbidden energy gap. Design equations for the forward and reverse characteristic of a diode are presented for several important cases. The breakdown voltage of the high voltage devices was shown to be a function of the width of the high resistivity region.

One unsolved problem is the surface limitation of breakdown voltage and reverse currents. This has been observed to decrease the breakdown voltages and increase the reverse currents to undesirable levels.

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